CLAIMS

What is claimed is:

1. A semiconductor package with enhanced electrical and thermal performance, comprising:

a substrate having a front surface and a back surface opposed to the front surface, wherein a plurality of I/O (input/output) vias, power vias and ground vias are formed to extend from the front surface to the back surface of the substrate;

at least a chip having an active surface and an inactive surface opposed to the active surface, wherein the active surface is formed with a plurality of I/O pads, power pads and ground pads, allowing the I/O pads to be electrically connected to the I/O vias of the substrate, and the active surface is further formed with a power plane and a ground plane in a manner that, the power plane is electrically connected to the power pads, and the ground plane is electrically connected to the ground pads; and wherein the inactive surface of the chip is mounted on the front surface of the substrate;

a power-connecting heat spreader mounted over the front surface of the substrate in a manner that, the power-connecting heat spreader entirely covers the chip, and is adapted to be electrically bonded to the power vias of the substrate and the power plane on the chip;

a ground-connecting heat spreader mounted over the front surface of the substrate to entirely cover the chip in a manner that, the ground-connecting heat spreader is positioned in elevation above the power-connecting heat spreader, and adapted to be electrically bonded to the ground vias of the substrate and the ground plane on the chip;

an encapsulation body for encapsulating the front surface of the substrate, the chip, the power-connecting heat spreader and the ground-connecting heat spreader; and

a plurality of solder balls implanted on the back surface of the substrate and electrically bonded to the vias.

2. The semiconductor package of claim 1, wherein the I/O pads are electrically connected to the I/O vias by means of wire-bonding technology.

3. The semiconductor package of claim 1, wherein the power plane and the ground plane are electrically connected respectively to the power pads and the ground pads by means of wire-bonding technology.

4. The semiconductor package of claim 1, wherein the power plane and the ground plane are electrically connected respectively to the power pads and the ground pads by means of TAB (tape automated bonding) technology.

5. The semiconductor package of claim 1, wherein the power-connecting heat spreader and the ground-connecting heat spreader are each an integrally-formed piece of electrically-and-thermally conductive material.

6. The semiconductor package of claim 1, wherein the power-connecting heat spreader includes a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion; the support portion is bonded to the power vias of the substrate, and the downward-extending portion is bonded to the power plane on the chip, allowing the overhead portion to be elevated in position above the chip by the support portion and the downward-extending portion in a manner that, the power-connecting heat spreader entirely covers the chip.

7. The semiconductor package of claim 6, wherein the ground-connecting heat spreader includes a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion; the support portion is bonded to the ground vias of the substrate, and the downward-extending portion is bonded to the ground plane on the chip, allowing the overhead por-

tion to be elevated by the support portion and the downward-extending portion in position above the overhead portion of the power-connecting heat spreader.

8. The semiconductor package of claim 7, wherein the overhead portion of the power-connecting heat spreader is formed with an opening, for allowing the downward-extending portion of the ground-connecting heat spreader to penetrate through the opening and to be electrically bonded to the ground plane on the chip.

9. The semiconductor package of claim 7, wherein the support portion of the power-connecting heat spreader and the support portion of the ground-connecting heat spreader are each formed with at least an opening, for allowing a molding compound used for forming the encapsulation body to pass through the opening.

10. A semiconductor package with enhanced electrical and thermal performance, comprising:

a substrate having a front surface and a back surface opposed to the front surface, wherein a plurality of I/O (input/output) vias, power vias and ground vias are formed to extend from the front surface to the back surface of the substrate;

at least a chip having an active surface and an inactive surface opposed to the active surface, wherein the active surface is formed with a plurality of I/O pads, power pads and ground pads, allowing the I/O pads to be electrically connected to the I/O vias of the substrate, and the active surface is further formed with a power plane and a ground plane in a manner that, the power plane is electrically connected to the power pads, and the ground plane is electrically connected to the ground pads; and wherein the inactive surface of the chip is mounted on the front surface of the substrate;

a power-connecting heat spreader having a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion, wherein the support portion is electrically bonded to the power vias of the substrate, and the downward-extending portion is electrically

bonded to the power plane on the chip, allowing the overhead portion to be elevated in position above the chip by the support portion and the downward-extending portion in a manner that, the power-connecting heat spreader entirely covers the chip;

a ground-connecting heat spreader having a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion, wherein the support portion is electrically bonded to the ground vias of the substrate, and the downward-extending portion is electrically bonded to the ground plane on the chip, allowing the overhead portion to be elevated by the support portion and the downward-extending portion in position above the overhead portion of the power-connecting heat spreader in a manner that, the ground-connecting heat spreader entirely covers the chip;

an encapsulation body for encapsulating the front surface of the substrate, the chip, the power-connecting heat spreader and the ground-connecting heat spreader, wherein the overhead portion of the ground-connecting heat spreader is exposed to outside of the encapsulation body; and

a plurality of solder balls implanted on the back surface of the substrate and electrically bonded to the vias.

11. The semiconductor package of claim 10, wherein the power-connecting heat spreader and the ground-connecting heat spreader are each an integrally-formed piece of electrically-and-thermally conductive material.

12. The semiconductor package of claim 10, wherein the overhead portion of the power-connecting heat spreader is formed with an opening, for allowing the downward-extending portion of the ground-connecting heat spreader to penetrate through the opening and to be electrically bonded to the ground plane on the chip.

13. The semiconductor package of claim 10, wherein the support portion of the power-connecting heat spreader and the support portion of the ground-connecting heat spreader

are each formed with at least an opening, for allowing a molding compound used for forming the encapsulation body to pass through the opening.

14. A method for fabricating a semiconductor package, comprising the step of:

preparing a substrate having a front surface and a back surface opposed to the front surface, wherein a plurality of I/O (input/output) vias, power vias and ground vias are formed to extend from the front surface to the back surface of the substrate;

mounting at least a chip having an active surface and an inactive surface opposed to the active surface, wherein the active surface is formed with a plurality of I/O pads, power pads and ground pads, and further formed with a power plane and a ground plane in a manner that, the power plane is electrically connected to the power pads, and the ground plane is electrically connected to the ground pads; and wherein the inactive surface of the chip is mounted on the front surface of the substrate;

forming a plurality of bonding wires for electrically connecting the I/O pads on the chip to the I/O vias of the substrate;

mounting a power-connecting heat spreader over the front surface of the substrate; the power-connecting heat spreader having a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion, wherein the support portion is electrically bonded to the power vias of the substrate, and the downward-extending portion is electrically bonded to the power plane on the chip, allowing the overhead portion to be elevated in position above the chip by the support portion and the downward-extending portion in a manner that, the power-connecting heat spreader entirely covers the chip;

mounting a ground-connecting heat spreader over the front surface of the substrate; the ground-connecting heat spreader having a support portion, an overhead portion supported on the support portion, and a downward-extending portion protruding downwardly from the overhead portion, wherein the support portion is electrically

bonded to the ground vias of the substrate, and the downward-extending portion is electrically bonded to the ground plane on the chip, allowing the overhead portion to be elevated by the support portion and the downward-extending portion in position above the overhead portion of the power-connecting heat spreader in a manner that, the ground-connecting heat spreader entirely covers the chip;

forming an encapsulation body for encapsulating the front surface of the substrate, the chip, the power-connecting heat spreader and the ground-connecting heat spreader; and

implanting a plurality of solder balls on the back surface of the substrate, and electrically bonding the solder balls to the vias.

15. The method of claim 14, wherein the power plane and the ground plane are electrically connected respectively to the power pads and the ground pads by means of wire-bonding technology.

16. The method of claim 14, wherein the power plane and the ground plane are electrically connected respectively to the power pads and the ground pads by means of TAB (tape automated bonding) technology.

17. The method of claim 14, wherein the power-connecting heat spreader and the ground-connecting heat spreader are each an integrally-formed piece of electrically-and-thermally conductive material.

18. The method of claim 14, wherein the overhead portion of the power-connecting heat spreader is formed with an opening, for allowing the downward-extending portion of the ground-connecting heat spreader to penetrate through the opening and to be electrically bonded to the ground plane on the chip.

19. The method of claim 14, wherein the support portion of the power-connecting heat spreader and the support portion of the ground-connecting heat spreader are each

formed with at least an opening, for allowing a molding compound used for forming the encapsulation body to pass through the opening.

20. The method of claim 14, wherein the overhead portion of the ground-connecting heat spreader is exposed to outside of the encapsulation body.

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